REMARKS

In the Office Action, the Examiner objected to the specification because no application numbers were listed for the referenced co-pending applications. The specification has been amended as indicated above. Applicant respectfully requests that the Examiner's objection to the specification be withdrawn.

Claims 1-53 are pending in the present application. In the Office Action, claims 1-2, 5-17, 21-24, 27-28, 32-34, 45-46, and 50-52 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Gafken (U.S. Patent No. 6,026,016). Claims 3-4, 18-20, 35, 41-42, and 53 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gafken in view of Short, "Embedded Microprocessor Design." The Examiner's rejections are respectfully traversed.

Independent claims 1, 35, 41-42, and 53 set forth Hardware-Debug-Test (HDT) enable bits that may be stored in a register and reset by a control logic. Claims 35, 41-42, and 53 set forth HDT enable bits that may be stored in a register and reset by a control logic and HDT enable lock bits.

Gafken describes a lock bit array 705 that includes a read lock bit, which may prevent a corresponding block from being accessed in response to a memory read operation directed to that block. The Examiner then alleges that a read operation is equivalent to a HDT operation. Applicant respectfully disagrees. HDT operations are well known in the art and persons of ordinary skill in the art will appreciate that simply preventing or allowing a memory read operation directed to a particular block of memory is not the same as enabling an HDT operation. Thus, Applicant submits that Gafken fails to teach or suggest HDT enable bits or HDT enable

lock bits. Accordingly, Applicant submits that the invention set forth in claims 1, 35, 41-42, 53, and all claims depending therefrom is not anticipated by Gafken.

Independent claim 16 sets forth one or more microcode loader enable bits that may be stored in a register and reset by a control logic. Claims 27 and 45 describe modifying microcode by receiving a request to modify microcode in determining a microcode loader enable status. Claims 32 and 50 describe changing a microcode loader enable status by receiving a request to change the microcode loader enable status and determining the status of a microcode loader enable lock.

Gafken describes a lock bit array 315 that includes a write lock bit, which indicates whether a corresponding block of memory is locked to prevent write or erase operations, or unlocked. A block of the memory array 130 that is write locked is prevented from being accessed for program or erase operations. See Gafken, col. 6, ll. 19-40. However, Gafken is completely silent with regard to enabling a microcode loader, *e.g.*, a unit or device that may load microcode. Accordingly, Applicant respectfully submit that the invention set forth in claims 16, 27, 32, 45, 50, and all claims depending therefrom is not anticipated by Gafken.

For at least the aforementioned reasons, Applicant requests that the Examiner's rejections of claims 1-2, 5-17, 21-24, 27-28, 32-34, 45-46, and 50-52 under 35 U.S.C. 102(b) be withdrawn

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the prior art of record. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Gafken is completely silent with regard to HDT enable bits or HDT enable lock bits (as set forth in claims 1, 35, 41-42, and 53) and enabling a microcode loader (as set forth in claims 16, 27, 32, 45, and 50). The Examiner

relies upon Short to describe using non-volatile memory to store data. However, Short fails to remedy the fundamental deficiencies of the primary reference. Neither Gafken nor Short is at all concerned with HDT enable bits or HDT enable lock bits (as set forth in claims 1, 35, 41-42, and 53) or enabling a microcode loader (as set forth in claims 16, 27, 32, 45, and 50). Accordingly, Applicant respectfully submits that the cited references also fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submits that the present invention is not obvious over Gafken and Short, either alone or in combination. Applicant requests that the Examiner's rejections of claims 3-4, 18-20, 35, 41-42, and 53 under 35 U.S.C. 103(a) be withdrawn.

In the Office Action, claims 25-26, 29-30, 36, 43-44, and 47-48 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Sakaki (U.S. Patent No. 5,826,007). Claims 31, 37-40, and 49 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Sakaki in view of Kime, "Logic and Computer Design Fundamentals." The Examiner's rejections are respectfully traversed.

Independent claims 25, 36, and 43 set forth receiving a request to initiate an HDT mode, determining a HDT mode enable status, and initiating the HDT mode if the HDT mode enable status is set to enabled. Independent claims 29 and 47 set forth receiving a request to change an HDT mode status, determining a HDT mode enable lock status, and modifying the HDT mode enable status if the HDT mode enable lock status is set to unlocked.

Sakaki describes a bus line control circuit 21 for protecting data in a test-only memory 17 and a ROM 12. However, Sakaki is completely silent with regard to a HDT mode. Consequently, Sakaki fails to teach or suggest receiving a request to initiate an HDT mode,

determining a HDT mode enable status, and initiating the HDT mode if the HDT mode enable status is set to enabled, as set forth in claims 25, 36, and 43. Sakaki also fails to teach or suggest receiving a request to change an HDT mode status, determining a HDT mode enable lock status, and modifying the HDT mode enable status if the HDT mode enable lock status is set to unlocked, as set forth in claims 29 and 47. The Examiner alleges that a HDT mode is discussed in Figure 4, step 230 in Sakaki. However, Sakaki does not include a Figure 4 and Applicant was unable to locate any mention of a HDT mode elsewhere in Sakaki. Accordingly, Applicant respectfully submit that the invention set forth in claims 25, 29, 36, 43, 47, and all claims depending therefrom is not anticipated by Sakaki.

For at least the aforementioned reasons, Applicant requests that the Examiner's rejections of claims 25-26, 29-30, 36, 43-44, and 47-48 under 35 U.S.C. 102(b) be withdrawn

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the prior art of record. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Sakaki is completely silent with regard to a HDT mode. The Examiner relies on Kime to describe uses of flip-flops. However, Kime fails to remedy the fundamental deficiencies of Sakaki.

For at least the aforementioned reasons, Applicant respectfully submits that the present invention is not obvious over Sakaki and Kime, either alone or in combination. Applicant requests that the Examiner's rejections of claims 31, 37-40, and 49 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the

undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 7/26/05

Mark W. Sincell, Ph.D.
Reg. No. 52,226
Williams Morgan & Amerson, P.C.
10333 Richmond Avenue, Suite 1100
Houston, TX 77042
(713) 934-7000
(713) 934-7011 (Fax)

AGENT FOR APPLICANTS